# CPCIserial-CAN/402-2

## CompactPCI® Serial (PCIe®) Board with 2 CAN Interfaces

**CompactPCI Serial Board with Altera® FPGA for 2x CAN via DSUB9 Connectors**

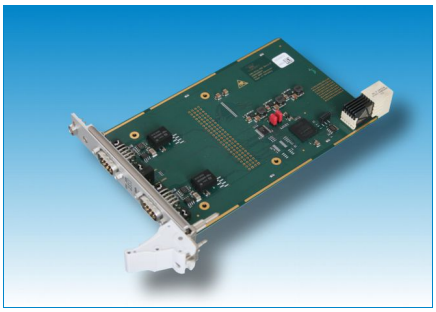
- High-speed CAN interfaces acc. to ISO 11898-2, bit rate up to 1 Mbit/s
- Bus mastering and local data management by FPGA (esdACC)
- PICMG® CPCI-S.0 standard supporting high-speed PCI Express® interface lines
- Selectable CAN termination on board and cut-out in the front panel for jumper view
- Supports MSI (Message Signaled Interrupts)

**Wide Range of OS Support and Advanced CAN Diagnostic**

- Software drivers for Windows® and Linux® included free of charge
- Optional CAN layer 2 software drivers for real-time operating systems
- CANopen®, J1939 and ARINC 825 protocol libraries
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology
- High resolution hardware timestamps

**Customization on Request**

- Ext. temperature range: -40° C … +75° C
- Error simulation support
- All signals via Rear I/O (P3)



**CAN Data Management**

The CPCIserial-CAN/402-2 is a CompactPCI Serial board with two electrically isolated high-speed CAN interfaces, according to ISO 11898-2, which are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core), implemented in the Altera FPGA. The FPGA supports bus mastering (firstparty DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load. Due to the usage of MSI the CPCIserial-CAN/402-2 can be operated for example in Hypervisor environments.
The CPCIserial-CAN/402-2 provides high resolution 64-bit hardware timestamps for CAN messages.

**Software Support**

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)
CAN layer 2 drivers for QNX, RTX(64), VxWorks® and On Time RTOS-32 can be ordered separately.

Higher Layer Protocols
Higher Layer Protocols are available for many operating systems (see order info):

- CANopen Master- and Slave-Stack
- J1939
- ARINC825

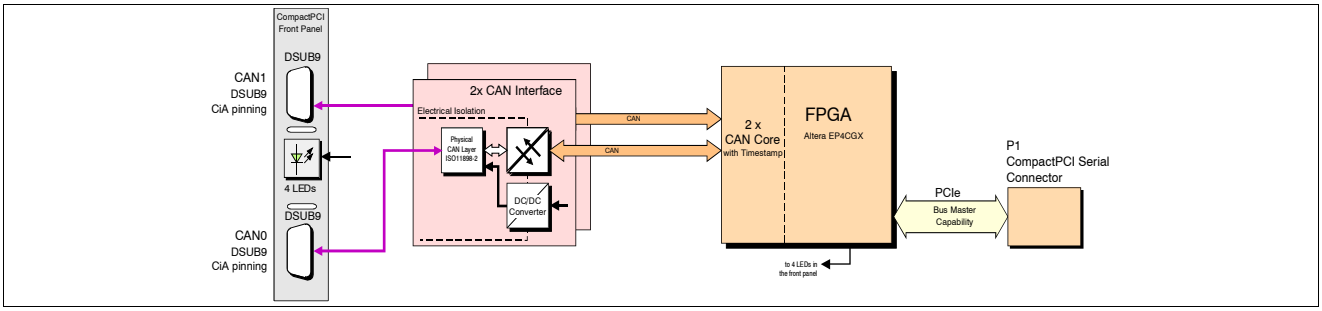
Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

**Customization on Request**

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.

**CPCIserial-CAN/402-2 Successors with CAN FD**

The CPCIserial-CAN/402-2 is not recommended for new designs. (It can still be used in existing systems, e.g. if the drivers shall not be reinstalled.)
Please use the successor CPCIserial-CAN/402-2-FD for new projects. If you need 4 CAN nets, use the CPCIserial-CAN/402-4-FD. Both CAN FD boards can also be used in Classical CAN applications, because they are fully backwards compatible.




**Technical Specifications:**

| | |
|---|---|
| *CompactPCI Serial Interface:* | |
| Interface | PICMG CPCI-S.0 Rev. 1.0, PCI Express Rev. 1.0a, Link width 1x |
| *CAN:* | |
| Interface | 2x high-speed CAN interfaces acc. to ISO 11898-2, bit rate up to 1 Mbit/s, CAN termination selectable via jumper, electrical isolation (1000 V, 1 s) |
| CAN controller | esdACC in EP4CGX Altera FPGA, acc. to ISO 11898-1 (CAN 2.0 A/B) |
| *General:* | |
| Ambient temp. | Operation: 0 °C ...+75 °C / Storage: -40 °C ...+85 °C |
| Rel. humidity | Max. 90 % (non-condensing) |
| Power supply | 12 V, 2x CAN $I_{MAX\_12V}$ = 200 mA, |
| Connector | CPCIserial: CompactPCI Serial connector P1, according to PICMG CPCI-S0 Rev. 1.0<br>CAN: DSUB9 |
| Weight | 150 g |
| Mechanics | 3 U / 4 HP, Compliant to IEEE 1101 |
| LEDs | 4x LEDs, CAN status, module status |
| Conformity | EN 61000-6-2, EN 61000-6-4, EMC, RoHS, CE |

*Order Information:*

| Hardware | | Order No. |
|---|---|---|
| CPCIserial-CAN/402-2 | 2x CAN via 2x DSUB9, 4 HP | I.3001.04 |

*Software Support*[1]

CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.

Additional CAN layer 2 object licenses including CD-ROM:

| | |
|---|---|
| CAN-DRV-LCD QNX | C.1101.32 |
| CAN-DRV-LCD VxWorks | C.1101.55 |
| CAN-DRV LCD RTX (incl. RTX64) | C.1101.35 |
| CAN-DRV LCD On-Time-RTOS-32 | C.1101.45 |
| Higher CAN layer protocols including CD-ROM: | |
| CANopen-LCD Windows/Linux, RTX, QNX or VxWorks | C.1101.xx |
| J1939 stack for Windows or Linux | C.1130.xx |
| ARINC 825-LCD for Windows/Linux, RTX, QNX or VxWorks | C.1140.xx |

*Related Products*

| | | |
|---|---|---|
| CPCIserial-CAN/402-2-FD | 2x CAN FD via 2x DSUB9, 4 HP | I.3001.64 |
| CPCIserial-CAN/402-4-FD | 4x CAN FD via 1x DSUB25, 4 HP | I.3001.68 |

[1] For detailed information about driver availability for your operating system please contact our sales team.

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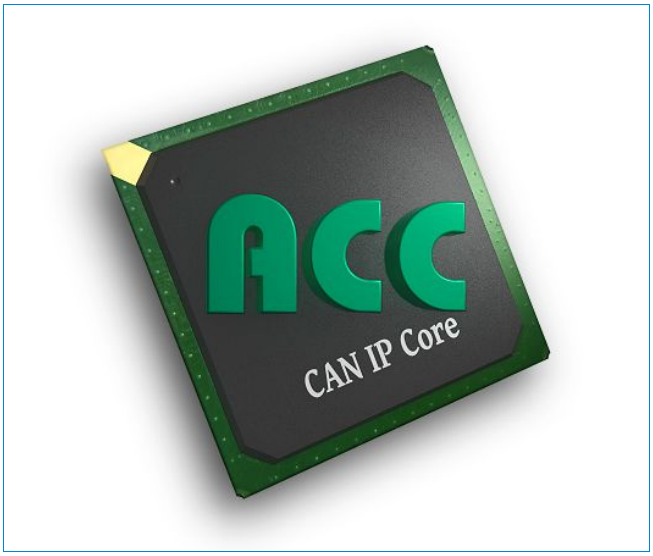
# CPCIserial-CAN/402-2

## Driven by esdACC (Advanced CAN Core)

### Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Test "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages )
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement




### Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - Timestamping complies with the CiA 603 specification
- TX FIFO (16 CAN frames deep )
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

### Superior esdACC Features (continued):

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction relieves the host CPU (needs bus master capable local bus to host interface) [1]
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Altera® Cyclone FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

*For further information on the esdACC IP Core please contact our sales team.*



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