CAN-PCI/402

1, 2 or 4 Channel PCI-CAN Interface (Layer 2, CANopen® or J1939)

PCI Board with High-Performance Altera® FPGA for up to 4x CAN

- *1x, 2x or 4x CAN interfaces according to ISO 11898-2*
- *Bus mastering and local data management by FPGA*
- *PCI interface according to PCI Local Bus Specification 3.0*
- *Selectable CAN termination on board*
- *Supports MSI (Message Signaled Interrupts)*

Wide Range of Operating System Support and Advanced CAN Diagnostic

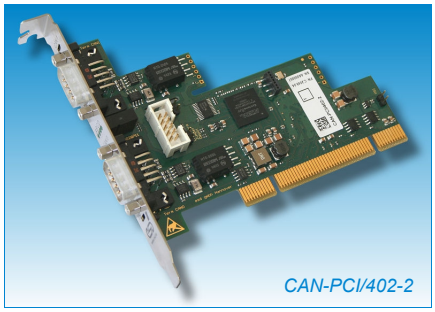
- *Software drivers for Windows® and Linux® included free of charge*
- *Optional CAN layer 2 software drivers for real-time operating systems*
- *CANopen®, J1939 and ARINC 825 protocol libraries available*
- *ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology*
- *High resolution hardware timestamps*

Variety of Product Designs

- *Product versions available with or without electrical isolation*
- *Low profile version for 1x CAN*

Customization on Request

- *Ext. temperature range: -40°C … 75°C*
- *Error simulation support*
- *4x CAN via DSUB37*



CAN-PCI/402-2

Wide Choice of Hardware Designs

The CAN-PCI/402 is a PC board designed for the PCI bus that features one, two (CAN-PCI/402-2) or four (CAN-PCI/402-4/2Slot) electrically isolated high-speed CAN interfaces according to ISO 11898-2.
The CAN-PCI/402-4/2Slot comes with two CAN interfaces via a separate slot bracket.
These product versions are also available without electrical isolation.
The board is also available as low profile version CAN-PCI/402-1-LP.

CAN Data Management

The independent CAN nets according to ISO 11898-1 are driven by the esdACC (esd Advanced CAN Core) implemented in the Altera FPGA. The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.
Due to the usage of MSI (Message Signaled Interrupts) the CAN-PCI/402 can be operated for example in Hypervisor environments.
The CAN-PCI/402 provides high resolution hardware timestamps.

Software Support[1]

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)
CAN layer 2 drivers, e.g.QNX® and RTX64®, can be ordered separately, others on request.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):

- *CANopen Master- and Slave-Stack*
- *J1939*
- *ARINC825*

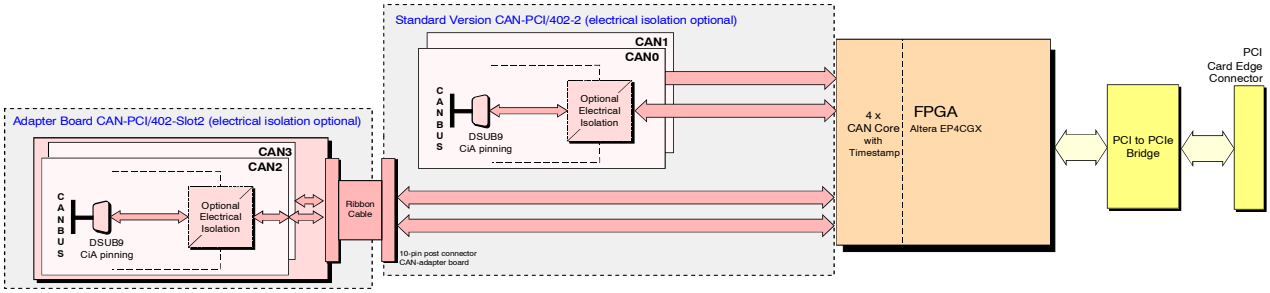
Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information. For example a PCI board with 4x CAN via 1x DSUB37 connector in the slot bracket is available on request.

Related Products

The CAN-PCI/402-2-FD is available with two CAN FD interfaces.



Technical Specifications:

PCI Interface:	
Specification	*PCI 3.0, 32 bit, 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability*

CAN:	
Interface	*1x, 2x or 4x CAN high-speed interfaces according to ISO 11898-2, bit rate up to 1 Mbit/s, with or without electrical isolation*
CAN controller	*esdACC in EP4CGX Altera FPGA, acc. to ISO 11898-1 (CAN 2.0 A/B)*

General:		
Ambient temp.	*0 °C ... +75 °C*	
Rel. humidity	*Max. 90 % (non-condensing)*	
Power supply	*3.3 V:*	*2x CAN I_{MAX} = 700 mA* *4x CAN I_{MAX} = 1.1 A*
Connector	*PCI:* *CAN:*	*PCI card edge connector* *1x 9-pin DSUB per CAN channel, male*
Weight	*CAN-PCI/402-2: 75 g*	

Order Information:

Hardware		*Order No.*
CAN-PCI/402-1	*1x CAN (CAN 1 only)*	*C.2049.02*
CAN-PCI/402-1-D	*as C.2049.02 but without electr. isolation*	*C.2049.03*
CAN-PCI/402-2	*2x CAN (CAN 1, CAN2)*	*C.2049.04*
CAN-PCI/402-2-D	*as C.2049.04 but without electr. isolation*	*C.2049.05*
CAN-PCI/402-4/2Slot	*4x CAN (C.2049.04, C.2045.10)*	*C.2049.06*
CAN-PCI/402-4-D/2Slot	*as C.2049.06 but without electr. isolation*	*C.2049.07*
CAN-PCI/402-1-LP	*Low profile version, CAN 1*	*C.2049.32*
Accessories		
CAN-PCIe/402-Slot2	*Adapter board, CAN 3,4, cable*	*C.2045.10*
CAN-PCIe/402-Slot2-D	*as C.2045.10 but without electr. isolation*	*C.2045.11*
Software Support[1]		
CAN layer 2 drivers for Windows and Linux are included in delivery.		
Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX		*C.1101.32*
CAN-DRV-LCD VxWorks		*C.1101.55*
CAN-DRV LCD RTX (incl. RTX64)		*C.1101.35*
Higher CAN layer protocols including CD-ROM:		
CANopen-LCD Windows/Linux, RTX, QNX or VxWorks		*C.1101.xx*
J1939 stack for Windows or Linux		*C.1130.xx*
ARINC 825-LCD for Windows/Linux, RTX, QNX or VxWorks		*C.1140.xx*

[1] *For detailed information about driver availability for your operating system please contact our sales team.*

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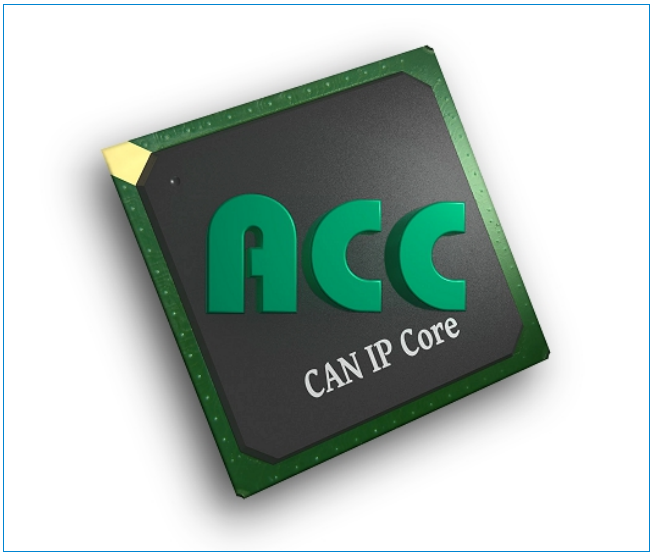
CAN-PCI/402

Driven by esdACC (Advanced CAN Core)

Basic Product Features:
• CAN ISO 11898-1 protocol compatibility
• Tested and certified acc. to ISO CAN Conformance Tests “ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan”
• 11-bit and 29-bit CAN IDs
• Bit rates from 10 kbit/s up to 1 Mbit/s supported
• Receive buffer (64 CAN messages)
• Complete access to CAN error counters
• Programmable error warning limit
• Error code capture register
• Error interrupt for each CAN bus error
• Arbitration lost interrupt with detailed bit position
• Listen only mode (no acknowledge, no active error flags)
• Automatic bit rate detection (hardware supported bit rate detection)
• Acceptance filter (4-byte code, 4-byte mask)
• Self reception mode (reception of ‘own’ messages)
• Busload measurement



Superior esdACC Features [1]:
• Operating system independently programmable via esd's NTCAN-API

• 32-bit register interface optimized for CAN needs
  • Easy to program
  • Transmission and reception of CAN frames with a minimum of register accesses

• RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  • Timestamping complies with the CiA 603 specification
  • On hardware with IRIG-B interfaces IRIG-B time is used for timestamping

• TX FIFO (16 CAN frames deep)
  • Providing the means to generate 100% busload even with non-realtime operating systems
  • Providing the means for real back-to-back transmission

• Timestamped Tx FIFO (16 CAN frames deep)
  • High priority
  • 64 bit timestamp
  • Bit time accuracy for CAN transmission

• Frame accurate abortion of transmissions with minimum delay
  • e.g. for driver timeouts
  • ISO11898-1 conform
  • Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:
• Hardware timer to provide accurate software timeouts beyond operating system accuracy
• Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
• Optional integration with 32-bit microcontroller to further relieve host CPU
• Optional different sources for timestamps (e.g. IRIG-B)
• Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
• The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

[1] *Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.*

For further information on the esdACC IP Core please contact our sales team.

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