CAN-M.2/402-2-FD

M.2 Card with 2 CAN FD Interfaces

Single Lane M.2 PCIe Card with Intel® FPGA for 2x CAN FD

- *2 CAN FD interfaces according to ISO 11898-2*
- *Bus mastering and local data management by FPGA*
- *Supports MSI (Message Signaled Interrupts)*
- *2280 or 2260 form factor with B & M-Key*

Wide Range of OS Support and Advanced CAN Diagnostic

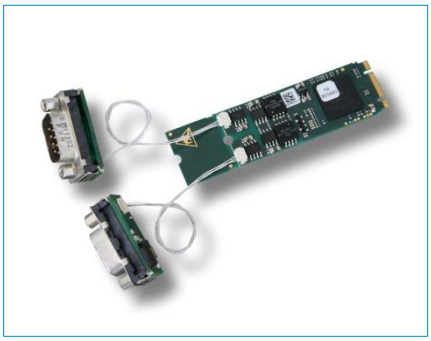
- *Software drivers for Windows® and Linux® included free of charge*
- *Optional CAN layer 2 software drivers for real-time operating systems*
- *CANopen®, J1939 and ARINC 825 protocol libraries (Classical CAN mode only)*
- *ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology*
- *High resolution hardware timestamps*

Flat Design of CAN Interface Adapter

- *Adapter with DSUB9 connector and selectable CAN termination on board*

Customization on Request

- *Version for extended operating temperature range: -40°C … +85°C*



Hardware Designs

The CAN-M.2/402-2-FD is an M.2 Card, that features two electrically isolated CAN FD interfaces.
The optional adapter CAN-PCIeMini/402-DSUB comes with a DSUB9 connector, selectable on-board CAN termination and an adapter cable.
CAN-M.2/402-2-FD is fully backwards compatible with CAN and can also be used in Classical CAN applications.

CAN Data Management

The independent CAN nets are driven by the ISO 16845:2004 certified esdACC (esd Advanced CAN Core) implemented in the Intel FPGA. The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory.
This results in a reduction of overall latency on servicing I/O transactions, in particular at higher data rates and a reduced host CPU load.
Due to the usage of MSI (Message Signaled Interrupts) the CAN-M.2/402-2-FD can be operated for example in Hypervisor environments.
The CAN-M.2/402-2-FD provides high resolution 64-bit hardware timestamps for CAN messages.

Software Support

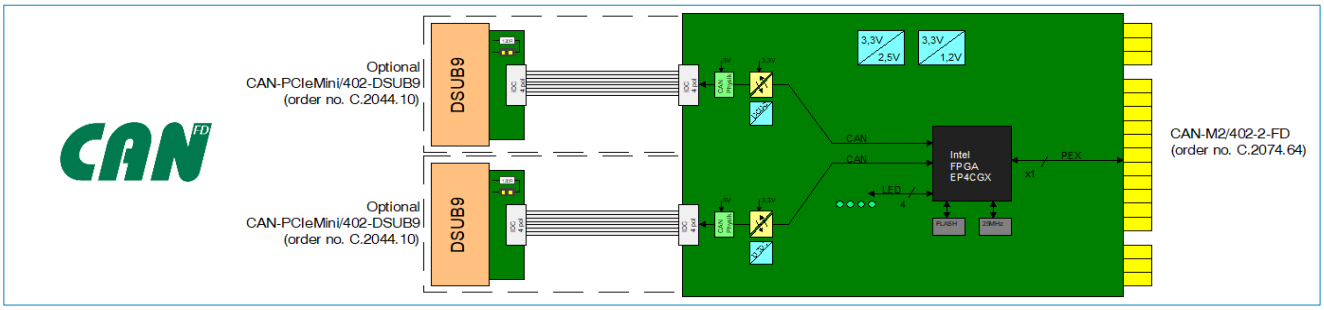
Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Real-time OS (NTCAN-API)
CAN layer 2 drivers e.g. for QNX® and RTX64® can be ordered separately.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):
• CANopen Master- and Slave-Stack
• J1939
• ARINC825

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.



Technical Specifications:

PCI Express Mini Interface:	
PCIe port	*PCI Express Spec. R1.0a, Link width 1x*
Form factor	*2280, can be reduced to 2260* *The component heights on the PCB top side exceed the requirements of the PCI Express M.2 specification. The maximum component height is 2.24 mm instead of 1.5 mm.*
CAN:	
Interface	*2 interfaces according to ISO 11898-2, electrical isolation, Bit rates from 10 Kbit/s up to 8 Mbit/s*
CAN controller	*esdACC in EP4CGX Intel FPGA, according to ISO 11898-1:2015*
General:	
Power supply	*3.3 V: 2x CAN, I_{MAX} = 320 mA, I_{TYP} = 270 mA*
Ambient temp.	*Standard range: 0 °C ... +75 °C*
Rel. humidity	*Max. 90 % (non-condensing)*
Dimensions	*22 mm x 80 mm x 4.4 mm (PCB is prepared for shortening to 22 mm x 60 mm x 4.4 mm by simply breaking off)*
Weight	*Board: approximately 8 g;* *Adapter: approximately 8 g each*
Connectors	*M.2: B & M-Key connector* *CAN: 2x Wire-to-board IDC connector, 4-pin;* *via adapter to: 1x 9-pin DSUB male per CAN channel*

Order Information:		
Hardware		*Order No.*
CAN-M.2/402-2-FD	*Active CAN Interface Card for M.2, 2x CAN, electrically isolated*	*C.2074.64*
Accessories		
CAN-PCIeMini/402-DSUB9	*Adapter to 1x DSUB9 connector, male, inclusive cable (C.2044.14)*	*C.2044.10*
CAN-PCIeMini/402-Cable	*Adapter cable, length: 150 mm*	*C.2044.14*
Software Support [1]		

CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.
Additional CAN layer 2 object licences including CD-ROM:

Additional CAN layer 2 object licences including CD-ROM:	
CAN-DRV-LCD QNX	*C.1101.32*
CAN-DRV-LCD RTX (incl. RTX64)	*C.1101.35*
Higher CAN layer protocols including CD-ROM for Classical CAN:	
CANopen-LCD Windows/Linux, QNX or RTX	*C.1101.xx*
J1939 stack for Windows or Linux	*C.1130.xx*
ARINC 825-LCD for Windows/Linux, QNX or RTX	*C.1140.xx*

1 For detailed information about driver availability for your operating system please contact our sales team.

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

CAN-M.2/402-2-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:
• CAN ISO 11898-1:2015 protocol compatibility
• Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
• 11-bit and 29-bit CAN IDs
• Supported bit rates: From 10 kbit/s up to 8 Mbit/s
• Receive buffer (64 CAN messages)
• Complete access to CAN error counters
• Programmable error warning limit
• Error code capture register
• Error interrupt for each CAN bus error
• Arbitration lost interrupt with detailed bit position
• Listen only mode (no acknowledge, no active error flags)
• Automatic bit rate detection (hardware supported bit rate detection)
• Self-reception mode (reception of 'own' messages)
• Busload measurement

Superior esdACC Features [1]:
• Operating system independently programmable via esd's NTCAN-API

• 32-bit register interface optimized for CAN needs
  • Easy to program
  • Transmission and reception of CAN frames with a minimum of register accesses

• RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  • Timestamping complies with the CiA 603 specification
  • On hardware with IRIG-B interfaces IRIG-B time is used for timestamping

• TX FIFO (16 CAN frames deep)
  • Providing the means to generate 100% busload even with non-real-time operating systems
  • Providing the means for real back-to-back transmission

• Timestamped Tx FIFO (16 CAN frames deep)
  • High priority
  • 64-bit timestamp
  • Bit time accuracy for CAN transmission

• Frame accurate abortion of transmissions with minimum delay
  • e.g. for driver timeouts
  • ISO11898-1:2015 conform
  • Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:
• Hardware timer to provide accurate software timeouts beyond operating system accuracy
• Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
• Optional different sources for timestamps (e.g. IRIG-B)
• Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
• The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

[1] *Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.*

For further information on the esdACC IP Core please contact our sales team.

esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu