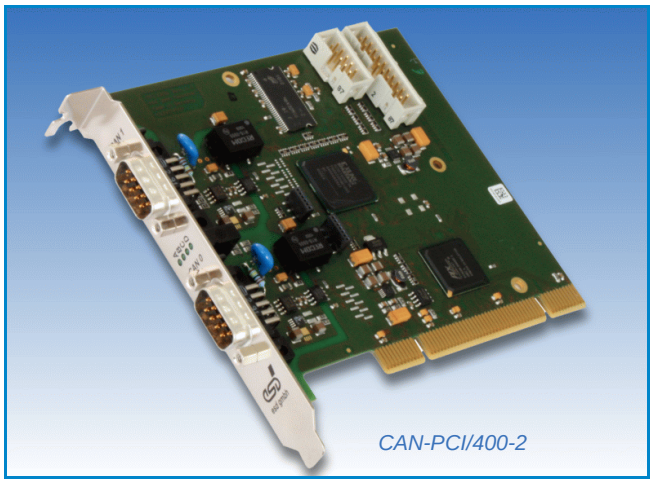
CAN-PCI/400

PCI-CAN Interface

- 2x or 4x High-Speed CAN interfaces according to ISO 11898-2
- Bus mastering and local data management by FPGA

- esd Advanced CAN Core (esdACC) technology
- PCI bus according to PCI Local Bus Specification 2.2

- Error simulation support
- Advanced CAN diagnostic



Powerful CAN Interface for PCs

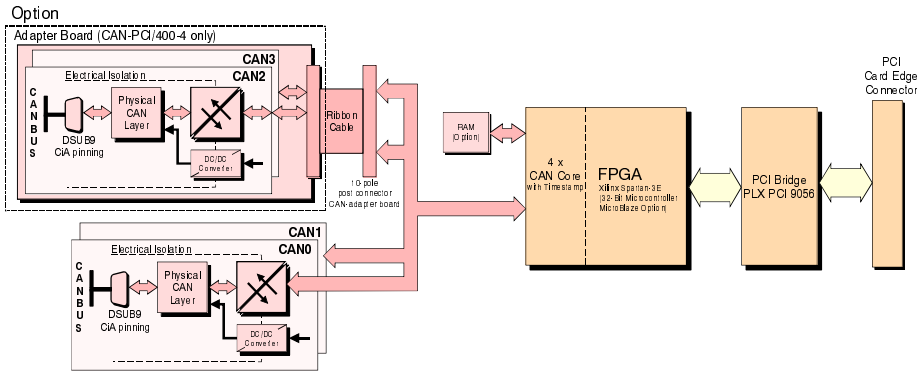
The CAN-PCI/400 is a PC board designed for the PCI bus that features two (CAN-PCI/400-2) or optionally four (CAN-PCI/400-4) electrically isolated CAN High-Speed interfaces according to ISO 11898-2. CAN-PCI/400-4 comes with two CAN interfaces via a separate slot bracket.

CAN Data Management

The independent CAN nets acc. to ISO 11898-1 are driven by the esdACC (esd Advanced CAN Core) implemented in the Xilinx Spartan 3e FPGA. Controlled by the FPGA the CAN-PCI/400 supports bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and reduced host CPU load.
The CAN-PCI/400 provides high resolution hardware timestamps. CAN Error injection on request.

Software Support [1]

CAN layer 2 (CAN-API) software drivers are available for Windows, VxWorks, QNX, RTX and Linux supporting up to 24 CAN nets. Drivers for other operating systems are available on request. The CANopen software package is available for Windows, VxWorks, Linux and QNX.



Technical Specifications:

PCI:	
Specification	*PCI 2.2, 32 bit 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability*
Memory	*BlockRAM: 72 KB, DDR-SDRAM: 64 MB*
Microprocessor	*Optional 32-bit µC in FPGA (MicroBlaze)*
CAN:	
Interface	*2x or optional 4x CAN high-speed interfaces according to ISO11898-2, differential, electrically isolated, bit rate up to 1 Mbit/s*
CAN controller	*esdACC in FPGA Spartan® 3e, acc. to ISO 11898-1 (CAN 2.0 A/B)*
General:	
Amb. temp.	*0...50 °C*
Humidity	*max. 90 %, non-condensing*
Connector	*CAN: DSUB9 male, PCI: PCI card edge connector*
LEDs	*CAN traffic, power*
Power Supply	*3.3 V / (depending on FPGA-image, 2x CAN: up to I = 1 A), and 5 V /250 mA*

Order Information:

Hardware		*Order No.*
CAN-PCI/400-2	*2x CAN version*	*C.2048.04*
CAN-PCI/400-4	*4x CAN version*	*C.2048.06*
CAN layer 2 drivers for Windows and Linux are included in delivery		
Software Support		
Additional CAN layer 2 object licences including CD-ROM [1]:		
CAN-DRV-LCD QNX		*C.1101.32*
CAN-DRV-LCD VxWorks		*C.1101.55*
CAN-DRV-LCD RTX		*C.1101.35*
Higher CAN layer protocols [1]:		
CANopen-LCD Windows/Linux		*C.1101.06*
CANopen-LCD QNX		*C.1101.17*
CANopen-LCD VxWorks		*C.1101.18*
CANopen-LCD RTX		*C.1101.16*
J1939 stack for Windows		*C.1130.10*
J1939 stack for Linux		*C.1130.11*
ARINC825-LCD Windows/Linux		*C.1140.06*
ARINC825-LCD RTX		*C.1140.16*
ARINC825-LCD QNX		*C.1140.17*
ARINC825-LCD VxWorks		*C.1140.18*

1 For detailed information about the driver availability for your operating system please contact our sales team.

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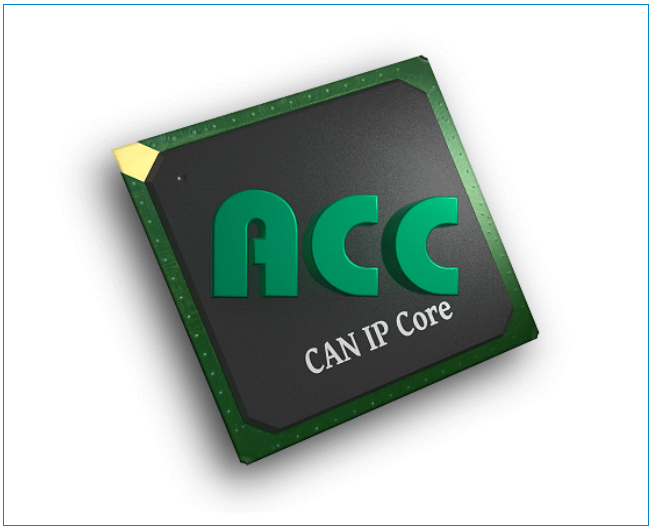
CAN-PCI/400

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-Bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)

Driver Availability:

Windows, Linux, QNX [1], VxWorks [1], RTX [1]

[1] For detailed information about the driver availability of your special operating system please contact our sales team.

Available higher level protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

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