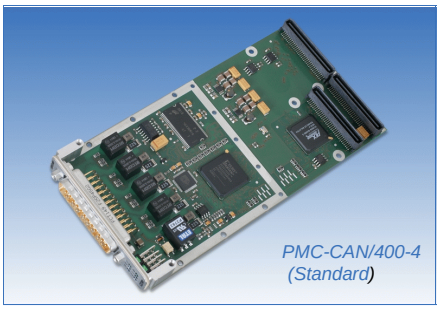
PMC-CAN/400-xx

4x CAN: Layer 2, CANopen or ARINC 825, optional IRIG-B

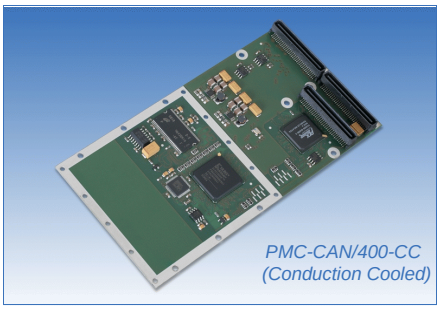
- 4 High-Speed CAN interfaces acc. to ISO 11898-2
- Bus mastering and local data management by FPGA (esdACC)

- PCI bus acc. to PCI Local Bus Specification 2.2
- ARINC 825 protocol available
- IRIG-B input (option)

- esd Advanced CAN Core (esdACC) technology
- Advanced CAN diagnostic
- Error simulation support
- All I/O-signals via 25-pin DSUB in the front panel
- Conduction cooled version available



PMC-CAN/400-4 (Standard)



PMC-CAN/400-CC (Conduction Cooled)

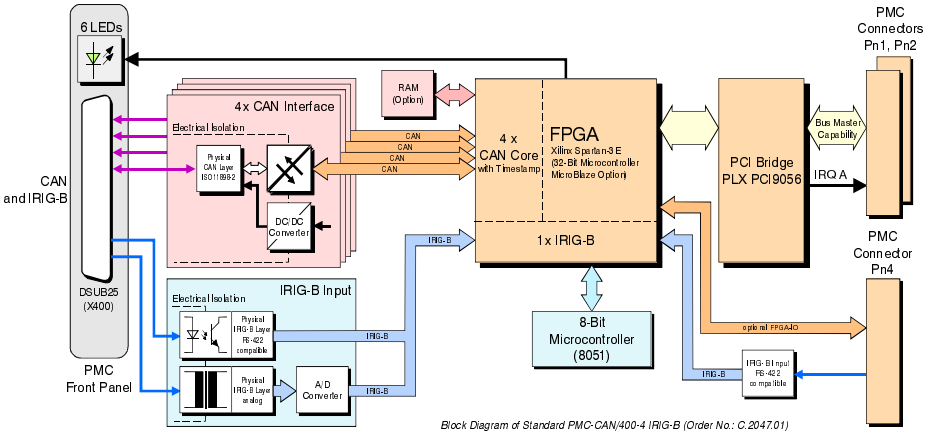
PMC CAN Interfaces
The PMC-CAN/400-4 features four electrically isolated CAN High-Speed interfaces according to ISO 11898.

CAN Data Management
The four independent CAN nets according to ISO 11898-1 are driven by the esd Advanced CAN Core (esdACC) CAN controller implemented in the Xilinx Spartan 3e FPGA.
Controlled by the FPGA the PMC-CAN/400-4 supports bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and reduced host CPU load.
The PMC-CAN/400-4 provides high resolution hardware timestamps.

IRIG-B
The IRIG-B interface offers inputs for analog or RS-422 IRIG-B coded signals. Both are electrically isolated. IRIG-B evaluation is controlled by an additional microcontroller.

Conduction Cooled Version
A conduction cooled version, the PMC-CAN/400-CC, is available. esd offers a VMEbus carrier board in conduction cooled design to carry up to two PMC-CAN/400-CC.

Software Support[1]
CAN layer 2 (CAN-API) software drivers are available for Windows, Linux, VxWorks, QNX and RTX, supporting up to 24 CAN nets.
The CANopen software package and ARINC 825 as another higher layer protocol are available for Windows, Linux, VxWorks, QNX and RTX. Drivers for other operating systems are available on request.



Block Diagram of Standard PMC-CAN/400-4 IRIG-B (Order No.: C.2047.01)

Technical Specifications:

PMC interface and Microprocessor:		
PCI	PCI 2.2, 32 bit 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability	
Memory	BlockRAM: 72 KB,	DDR-SDRAM: 64 MB
Microprocessor	optional 32-bit µC in FPGA (MicroBlaze)	
CAN:		
Interface	4x CAN high-speed interface acc. to ISO11898-2, differential, electrically isolated, bit rate up to 1 Mbit/s	
CAN controller	esdACC in FPGA Spartan® 3e, acc. to ISO 11898-1 (CAN2.0A/B)	
IRIG-B Input:		
Interface	1x analog and 1x RS-422 compatible (both electr. isolated), 1x RS-422 compatible (at PN4 only)	
Controller	8051 microcontroller	
General:		
Ambient temp.	Standard:	0 ...+50 °C (PMC-CAN/400-4)
	Extended:	-20...+75 °C (PMC-CAN/400-4-T)
	Conduction cooled:	-40...+85 °C (PMC-CAN/400-CC)
Humidity	Max. 90 %, non-condensing	
Power supply	5 V, 3.3 V	
Connectors	Pn1, Pn2, Pn4, DSUB25 (male, only C.2047.01 ... 03)	
LEDs:	4x CAN status, 1x IRIG-B, 1x module status (C.2047.01 ... 03)	

Order Information:		
Hardware		Order No.
PMC-CAN/400-4 IRIG-B	4x CAN, 1x IRIG-B, standard temp. range	C.2047.01
PMC-CAN/400-4-T	4x CAN, 1x IRIG-B, extended temp. range	C.2047.02
PMC-CAN/400-4	4x CAN, standard temp. range	C.2047.03
PMC-CAN/400-CC	as C.2047.01, but conduction cooled, interfaces available at Pn4 with TTL level only	C.2047.04
Accessories		
CAN/400-4-1C5	Adapter cable DSUB25 to 5x DSUB9	C.2047.18
CAN/400-4-1C4	Adapter cable DSUB25 to 4x DSUB9	C.2047.19
Software Support		
CAN layer 2 object licences including CD-ROM[1]:		
CAN-DRV-LCD Windows/Linux		C.1101.02
CAN-DRV-LCD VxWorks		C.1101.55
CANopen object licences including CD-ROM[1]:		
CANopen-LCD Windows/Linux		C.1101.06
CANopen-LCD VxWorks		C.1101.18
ARINC 825 object licences including CD-ROM[1]:		
ARINC825-LCD Windows / Linux		C.1140.06
ARINC825-LCD VxWorks		C.1140.18

1 For detailed information about the driver availability for your operating system please contact our sales team.

I:\Texte\Doku\DBL\PMC\Englisch\BLUE\PMC-CAN400-4_Datasheet_en_17.wpd

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

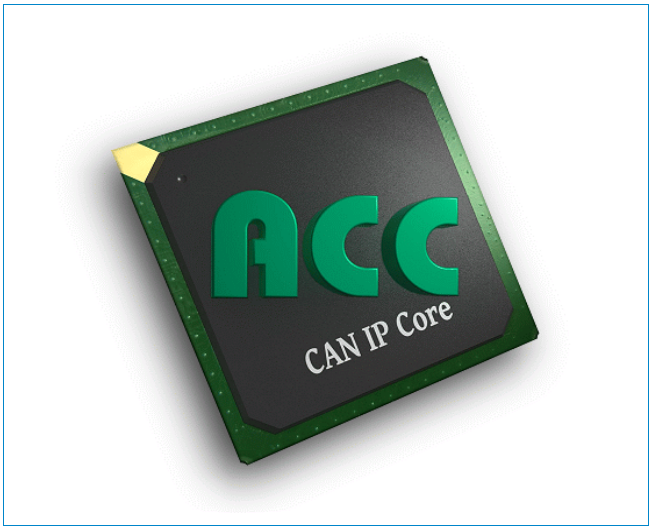
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

PMC-CAN/400-4

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-Bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)

Driver Availability:

Windows, Linux, QNX [1], VxWorks [1], RTX [1]

[1] For detailed information about the driver availability of your special operating system please contact our sales team.

Available higher level protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu