CAN-PCIe/402

PCI Express® Board with up to 4 CAN Interfaces

Single Lane PCIe Board with Altera FPGA for up to 4x CAN

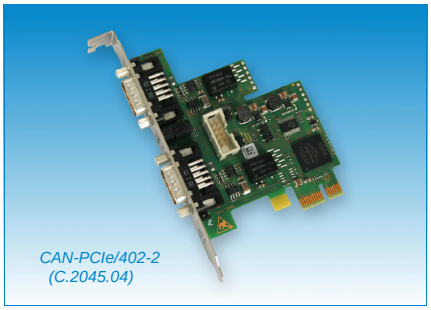
- *1x, 2x or 4x CAN interfaces according to ISO 11898-2*
- *Bus mastering and local data management by FPGA*
- *PCIe® interface according to PCI Express Specification R1.0a*
- *Selectable CAN termination on board*
- *Supports MSI (Message Signaled Interrupts)*

Wide Range of Operating System Support and Advanced CAN Diagnostic

- *Drivers and higher layer protocols for Windows®, Linux®, VxWorks®, QNX®, RTX, RTX64 and others*
- *CANopen®, J1939 and ARINC 825 protocols available*
- *esd Advanced CAN Core (esdACC) technology*

Variety of Product Designs

- *Product versions available with or without electrical isolation*
- *Low profile version for 1x CAN or 2x CAN*
- *4x CAN via 1x DSUB37 connector*



CAN-PCIe/402-2 (C.2045.04)

Wide Choice of Hardware Designs

The CAN-PCIe/402 is a PC board designed for the PCIe bus that features one, two (CANPCIe/402-2) or four (CAN-PCIe/402-4/2Slot) electrically isolated CAN High-Speed interfaces according to ISO 11898-2. The CAN-PCIe/402-4/2Slot comes with two CAN interfaces via a separate slot bracket. These product versions are also available without electrical isolation.

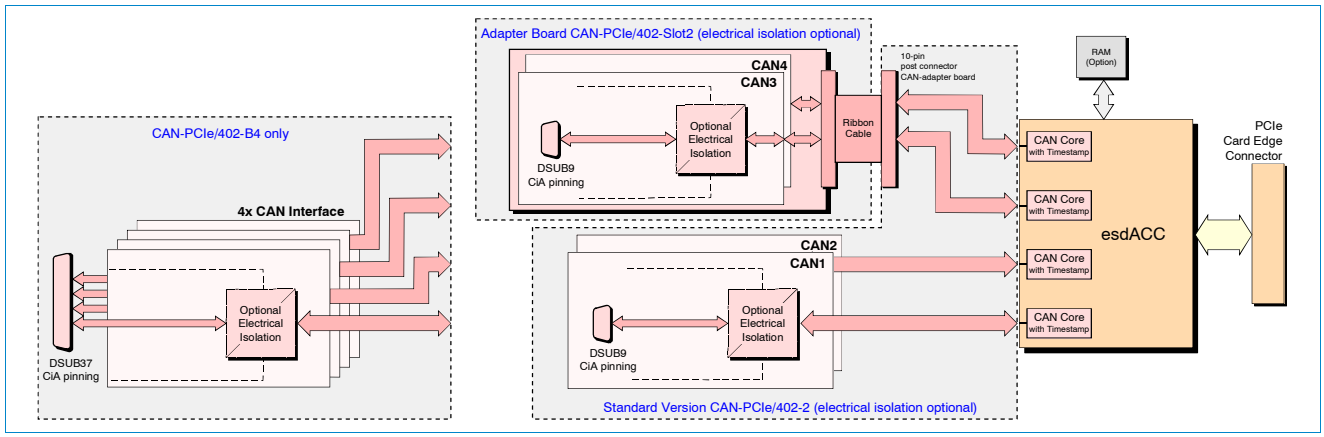
In the CAN-PCIe402-B4/1Slot version all four CAN interfaces are connected via one 37-pin DSUB connector.
Equipped with up to two CAN interfaces the board is available as low profile versions (CAN-PCIe/402-1-LP and -LP2).

CAN Data Management

The independent CAN nets according to ISO 11898-1 are driven by the esdACC (esd Advanced CAN Core) implemented in the Altera FPGA. Controlled by the FPGA the CAN-PCIe/402 supports bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and reduced host CPU load.
The CAN-PCIe/402 provides high resolution hardware timestamps.

Software Support[1]

CAN layer 2 (CAN-API) software drivers are available for Windows, Linux, VxWorks, QNX, RTX and RTX64. The CANopen software package is available for Windows, Linux, VxWorks and QNX.
Drivers for other operating systems are available on request.



Technical Specifications:

PCI Express Interface:	
PCIe port	*PCI Express Spec. R1.0a, Link width 1x*
CAN:	
Interface	*1x, 2x or 4x CAN high-speed interfaces according to ISO 11898-2, bit rate up to 1 Mbit/s, with or without electrical isolation*
CAN Controller	*esdACC in EP4CGX Altera FPGA, acc. to ISO 11898-1 (CAN 2.0 A/B)*
General:	
Ambient temp.	*0 °C ... +75 °C*
Rel. humidity	*Max. 90 % (non-condensing)*
Power Supply	*3.3 V: 2x CAN I_{MAX} = 280 mA, 4x CAN I_{MAX} = 290 mA* *12 V: 2x CAN I_{MAX} = 180 mA, 4x CAN I_{MAX} = 230 mA*
Connector	*PCIe: PCIe card edge connector* *CAN: 1x 9-pin DSUB per CAN channel, male (all except C.2045.08), 1x 37-pin DSUB, male (only C.2045.08)*
Weight	*CAN-PCIe/402-2: 60g*

Order Information:

Hardware		*Order No.*
CAN-PCIe/402-1	*1x CAN (CAN 1 only)*	*C.2045.02*
CAN-PCIe/402-1-D	*as C.2045.02 but without electr. isolation*	*C.2045.03*
CAN-PCIe/402-2	*2x CAN (CAN 1, CAN2)*	*C.2045.04*
CAN-PCIe/402-2-D	*as C.2045.04 but without electr. isolation*	*C.2045.05*
CAN-PCIe/402-4/2Slot	*4x CAN (C.2045.04, C.2045.10)*	*C.2045.06*
CAN-PCIe/402-4/2Slot-D	*as C.2045.06 but without electr. isolation*	*C.2045.07*
CAN-PCIe/402-B4/1 Slot	*4x CAN via 1x DSUB37, 1 Slot*	*C.2045.08*
CAN-PCIe/402-Slot2	*Adapter board, CAN 3,4, cable*	*C.2045.10*
CAN-PCIe/402-Slot2-D	*as C.2045.10 but without electr. isolation*	*C.2045.11*
CAN-PCIe/402-1-LP	*Low profile version, CAN 1*	*C.2045.32*
CAN-PCIe/402-1-LP-2	*Low profile version, CAN 2*	*C.2045.34*

CAN layer 2 drivers for Windows and Linux are included in delivery.

Software Support [1]	
Additional CAN layer 2 object licences including CD-ROM:	
CAN-DRV-LCD QNX	*C.1101.32*
CAN-DRV-LCD VxWorks	*C.1101.55*
CAN-DRV LCD RTX (incl. RTX64)	*C.1101.35*
Higher CAN layer protocols including CD-ROM:	
CANopen-LCD for Windows/Linux, RTX, QNX or VxWorks	*C.1101.xx*
J1939 stack for Windows or Linux	*C.1130.xx*
ARINC 825-LCD for Windows/Linux, RTX, QNX or VxWorks	*C.1140.xx*

[1] For detailed information about the driver availability for your operating system please contact our sales team.

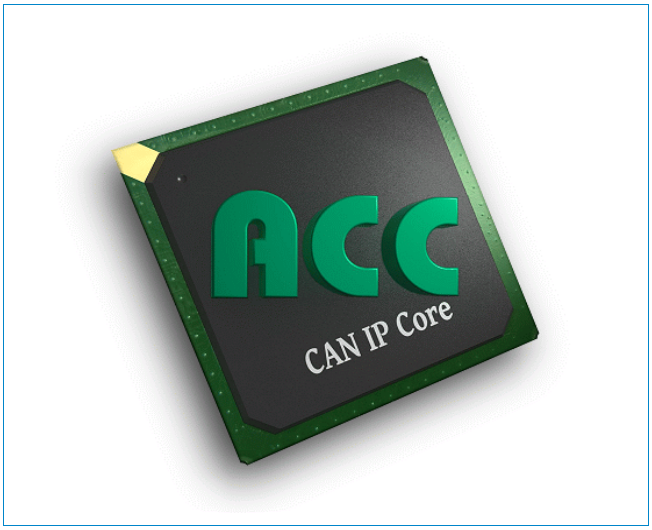
esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
Email: info@esd.eu

CAN-PCIe/402

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

Driver Availability:

Windows, Linux[1], QNX[1], VxWorks[1], RTX[1]

[1] For detailed information about the driver availability for your operating system and the particular esd CAN interface please contact our sales team.

Available Higher Level Protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

Availability of the superior esdACC features depends on the operating system and the hardware. Please contact our sales team for further information.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
Email: info@esd.eu