AMC-ADIO24 / AMC-ADIO24-HD50
AdvancedMC™ Analog/Digital I/O Module

Large Variety of High Speed and High Resolution I/Os on a Single Board
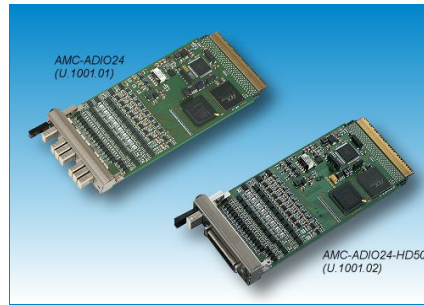- 8 analog inputs ±10 V, 16 bit, 200 KHz
- 2 analog outputs ±10 V, 16 bit, 600 KHz
- 24 digital I/Os, TTL level
- 4 trigger I/Os (RS-485)
- DMA to host CPU's memory to minimize latency for PCIe® read cycles

Two Different Connector Designs to Meet Individual Customer Requirements
- AMC-ADIO24 with 7x 10-pin Harting® har-link® connectors
- AMC-ADIO24-HD50 with 1x 10-pin har-link and 1x 50-pin har-mik® connectors

'Timing Routing Pool'
- Versatile trigger-conditions
- Prepared for MTCA.4 (MicroTCA® Enhancements for Rear I/O and Precision Timing)

AMC-ADIO24 (U.1001.01)

AMC-ADIO24-HD50 (U.1001.02)
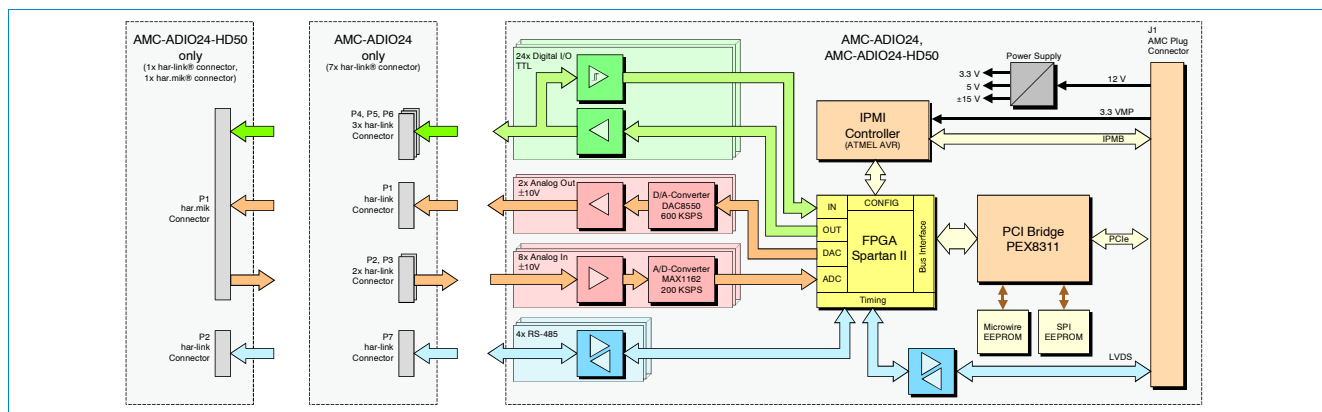
I/O Data Management
The AMC-ADIO24/-HD50 is equipped with a Spartan® FPGA that manages the I/O data exchange in cooperation with the PCIe bridge. FIFOs for input and output direction and DMA to the PCIe host CPU's memory minimize undesired latency during PCIe read cycles at higher data rates.
Read cycles of the PCIe CPU are reduced to setup and diagnosis tasks.

8 Analog Inputs with 16 Bit Resolution
The eight overvoltage protected analog inputs are connected to eight 16 bit A/D converters with a sampling rate of up to 200 kHz each.

2 Analog Outputs with 16 Bit Resolution
Both 16 bit analog outputs have a differential and a single ended output circuit, accessible at separate pins.
The outputs are transient and short circuit protected.

24 Digital I/Os with Programmable Output Configuration
Each of the 24 TTL-level I/Os can be separately configured as input or output. The outputs can be configured as high side driver, low side driver or both (sink/source). The I/O port's state can be read back in any configuration via a comparator with hysteresis.

Trigger I/Os for Synchronisation
The firmware offers a so called 'Timing Routing Pool' with various trigger conditions (RS-485 trigger input, timer, software, free flow) that can be individually evaluated for each I/O.

PCIe Device Access
For setup and I/O data exchange a comprehensive register description is available.

Technical Specifications:

MicroTCA/AMC Standards:

µTCA	PICMG® MTCA.0 R1.0, PICMG AMC.0 R2.0
IPMI	IPMI V1.5, controller Atmel® AVR
Updates	PICMG HPM.1 R1.0
PCIe bridge	PCISIG® PCIe spec. R.1.0a

Process Interfaces:

I/O control	FPGA Spartan II
Analog inputs	8 inputs, ±10 V, 16 bit resolution, up to 200 kHz sampling rate
Analog outputs	2 outputs, ±10 V, 16 bit resolution, up to 600 kHz update rate
Digital I/Os	24 I/Os, TTL level , programmable as input only, output sink, output source, output sink/source, max. current/channel: 64 mA sink, 32 mA source, up to 1 MHz input sampling rate, up to 1 MHz output update rate
Trigger ports	4 RS-485 ports, trigger/sync, max. 1 MHz

General:

Power supply	3.3 V ($I_{3.3VMPMAX}$= 60 mA), 12 V ($I_{12VTYPICAL}$ = 0.6 A, I_{12VMAX}= 1.0 A)
Ambient temp.	0 ...+70 °C (free convection)
Humidity	Max. 90 %, non-condensing
Dimensions	Single Mid-size AdvancedMC Module (73.8x18.96x181.5 mm)
Connectors	J1: AMC B/B+ compatible (MicroTCA)
	AMC-ADIO24: P1 ... P7: 10-pin har-link (I/Os)
	AMC-ADIO24-HD50: P1: 50-pin har-mik (I/Os) P2: 10-pin har-link (I/Os)
LEDs	Blue (hot plug), red (IPMI), green (OK)

Order Information:

Hardware		Order No.
AMC-ADIO24	8x AIN, 2x AOUT, 24x DIO and 4x trigger via 7x 10-pin har-link connector	U.1001.01
AMC-ADIO24-HD50	8x AIN, 2x AOUT, 24x DIO via 1x 50-pin har-mik connector and 4x trigger via 1x 10-pin har-link connector	U.1001.02